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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,481	04/14/2004	Vaishnav Srinivas	030333	8117

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EXAMINER	
TON, MY TRANG	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 05/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,481	SRINIVAS ET AL.	
	Examiner	Art Unit	
	My-Trang N. Ton	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-12,14-23 and 25-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-12,14-23 and 25-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner. for examination purposes only

10)☒ The drawing(s) filed on *14 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

MY-TRANG NU TON
PRIMARY EXAMINER

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

In response to Applicant's amendment filed on 2/22/06, the rejection made in the last Office action on the Wilford reference is withdrawn. A new Office action has been made as follows:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-5, 7-8 and 23-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Hong et al (U.S. Patent No. 6,933,755).

Hong et al discloses in fig. 3 a driver circuit including:

Regarding claim 1:

a driver (320) configured to switch a current source and a current sink to a load via a single node (node between PM5, NM5); and

a predriver (300) having first and second cross-coupled inverters (PM3, MP4, NM3, NM4) responsive to an input signal (INPUT SIGNAL), the first inverter (PM3, NM3) being configured to control the switching of the current source to the load and the second inverter (PM4, NM4) being configured to control the switching of the current sink

to the load, wherein the cross-coupling (300) between the first and second inverters and buffer connections of the first and second inverters to the driver (320) are configured such that the first inverter (PM3, MP4) controls the driver (320) to removes the current source from the load via the single node (the node between PM5, NM5) before the second inverter (PM4, NM4) controls the driver (320) to switch the current sink to the load via said single node (the node between PM5, NM5) in response to a transition in the input signal (INPUT SIGNAL) such that a crow-bar current is controlled, and conversely the second inverter (PM4, NM4) controls the driver (320) to removes the current sink from the load via said single node (the node between PM5, NM5) before the first inverter (PM3, NM3) controls the driver (PM5, NM5) to switch the current source to the load via said single node (the node between PM5, NM5) in response to an opposite transition in the input signal (INPUT SIGNAL) such that the crow-bar current is controlled, and wherein the first and second inverters (PM3, PM4, NM3, NM4) are further configured to remove both the concurrently source and the current sink from the load concurrently to allow tristate operation of the driver (320). Because the structure of the claim is fully met so the functional limitation recited therein is also met.

Regarding claim 2: each of the inverters comprises a pair of transistors connected in series (PM3, PM4, NM3, NM4).

Regarding claim 3: each of the transistors (PM3, PM4, NM3, NM4) comprises a field effect transistor (FET).

Regarding claim 4: each of the inverters comprises a p-channel FET (PM3, PM4) having a drain and an n-channel FET (NM3, NM4) having a drain connected to the drain of the PFET (PM3, PM4).

Regarding claim 5: for each of the inverters, the NFET (NM3, NM4) comprises a gate responsive to the input signal (INPUT SIGNAL), and the PFET (PM3) comprises a gate coupled to the drain of the PFET (PM4) in the other inverter.

Regarding claim 7: Hong et al is silent about size for transistors PM3, PM4, NM3, NM4, thus assume NM3=NM4 in size and PM3=PM4 in size.

Element VDD reads on a voltage source as recited in claim 8.

Regarding claim 23:

inverter means (INV6) for receiving an input signal (output of INV5) and inverting the input signal;

cross-coupled inverter means (300) for providing a break-before-make delay, wherein the cross-coupled inverter means (300) is configured to receive the output of the inverter means (INV6), and the cross-coupled inverter means is further configured to receive the input signal (the output of INV5 via TG1);

first and second output buffer means (INV7-INV9) for receiving first and second outputs (CP1, CP2) of the cross-coupled inverter means (300), for inverting (INV7) the first output (CP1) of the cross-coupled inverter means (300) while leaving the second output (CP2) of the cross coupled inverter means (300) uninverted (due to INV8, INV9) so that the first output buffer means (INV7) provides a break transition before the second output buffer means (INV8-INV9) provides a make transition, and the second

output buffer means (INV8-INV9) provides a break transition before the first output buffer means.(INV7) provides a make transition; and

first and second tristate means (NAND3, NOR, see fig. 6) for disabling output signals of the first and second predriver output nodes.

Element VDD reads on voltage supply means as recited in claim 25.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hong as applied to claim 1 above.

As stated above, every element of the claimed invention recited in above claims can be seen in the circuit of Hong. However, this reference does not show the "NFET is larger than the PFET" as recited in claim 6.

Although Hong does not expressly state the size value for the transistors, this difference is not of patentable merit because it is notoriously well known in the art that different sizes for the transistors can be selected in order to produce correspondingly different output values. Clearly, if designer wish to triggering faster and improving circuit reliability, there is well-known way to do such as: increasing the size for the transistor NM3, NM4 and decreasing the size for transistors PM3, PM4.

Claims 10-12, 14-22 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hong.

Claim 10 is similarly rejected as above claims:

an input inverter (INV6) configured to receive an input signal (output of INV5);

two cross-coupled inverters that include a first and second NFET (NM3, NM4) and a first and second PFET (PM3, PM4), wherein the first NFET is configured to receive the output of the input inverter (INV6), and wherein the second NFET is configured to receive the input signal (the output of INV5 via TG1);

first and second output buffers (INV7-INV9) configured to receive first and second outputs (CP1, CP2) of the two cross-coupled inverters (PM3, PM4, NM3, NM4), wherein the first buffer (INV7) inverts the first output (CP1) and the second buffer (INV8-INV9) leaves the second output (CP2) uninverted;

first and second tristate devices (NAND3, NOR, see Fig. 6) configured to disable output signals of the first and second predriver output nodes.

Moreover, the same motivation applied to claim 6 is applied to claim 10 regarding the limitation "the NFETs of the cross coupled inverters are larger than the PFETs of the cross-coupled inverters": if designer wish to triggering faster and improving circuit reliability, there is well-known way to do such as: increasing the size for the transistor NM3, NM4 and decreasing the size for transistors PM3, PM4.

The limitation recited in claim 11 is inherently seen in Hong (due to the structure is fully met).

Regarding claim 12: Hong et al is silent about size for transistors PM3, PM4 thus assume PM3=PM4 in size.

Each tristate device is a logic gate (NAND3, NOR) as recited in claim 14.

The first tristate device is a NAND gate (NAND3) and the second tristate device is a NOR gate (NOR) as recited in claim 15.

The first tristate device is an NFET (NAND3 includes NFET) and the second tristate device is a PFET (NOR includes PFET) as recited in claim 16.

Elements PM5-NM5 read on the output driver device and a capacitive load (inherently seen connected to OUTPUT DRIVING UNIT) as recited in claim 17.

Regarding claim 18: each of the input inverter (INV6), the cross-coupled inverters (PM3, PM4, NM3, NM4) and the fist and second output buffers (INV7-INV9) are further sized so as to be sufficiently large to drive the capacitive load (inherently seen connected to OUPUT DRIVING UNIT).

The output driver device includes an NFET device (NM5) and a PFET device (PM5) as recited in claim 19.

Element VDD reads on a voltage supply as recited in claim 20.

The voltage supply (VDD) is coupled between the first and second PFETs (PM3, PM4) of the cross-coupled inverter as recited in claim 21.

The output buffers include one or more inverters (INV7-INV9) as recited in claim 22.

The method recited in claims 26-27 are similarly rejected as claims 10 and 18.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

My-Trang N. Ton
Primary Examiner
Art Unit 2816

April 28, 2006